Jonathan Bailey

Contact

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Research Interests

Computer Architecture, Compilers, Hardware / Software Co-Design, and Throughput Processors

Education

Ph.D. Computer Science and Engineering 09/2015-Present
University of Michigan Ann Arbor, MI
Advisor: Prof. Scott Mahlke
Cumulative GPA: 4.0

M.S. Computer Science and Engineering 09/2015-12/2016
University of Michigan Ann Arbor, MI
Cumulative GPA: 4.0

B.S. Computer Engineering 08/2011-05/2015
Clemson University Clemson, SC
Cumulative GPA: 4.0

Publications

Scratch That (But Cache This): A Hybrid Register Cache / Scratchpad for GPUs
Jonathan Bailey, John Kloosterman, Scott Mahlke
International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES) 2018

RegLess: Just-in-Time Operand Staging for GPUs
John Kloosterman, Jonathan Beaumont, D. Anoushe Jamshidi, **Jonathan Bailey**, Trevor Mudge, Scott Mahlke
International Symposium on Microarchitecture (MICRO) 2017

Experience

University of Michigan 05/2016-Present
Graduate Student Research Assistant Ann Arbor, MI

- Currently investigating dynamic compilation and hardware reconfiguration
- Previously researched GPU register caching techniques and developed a hybrid register cache / scratchpad

Arm 05/2017-9/2017
Media Processing Group Intern San Jose, CA

- Explored methods to reduce GPU register file power

The Boeing Company 05/2014-08/2014
Information Technology Intern Renton, WA

- Developed an Android application for navigating to Boeing facilities
- Investigated a possible implementation of a proposed alert application for Android wearables

Clemson University 05/2013-06/2013
Research Assistant Clemson, SC

- Explored 3D printing capabilities with multidisciplinary engineering team
- Developed a method to send remote printer alerts to users

Course Projects

Acceleration of Pruned Neural Networks on GPUs Winter 2016
EECS 570, Parallel Computer Architecture

- Identified characteristics of GPUs that prevent them from translating the reduced structure of pruned neural networks into improved performance
- Proposed and evaluated architectural modifications that allow performance to scale more effectively with neural network pruning

Superscalar Out-of-Order Processor Fall 2015
EECS 470, Computer Architecture

- Designed a synthesizable DEC Alpha out-of-order processor in Verilog
- Incorporated advanced features such as three-way issue, a load-store queue, instruction prefetching, early tag broadcast, and a branch predictor with a return address stack
- Achieved the fastest single-threaded performance in the class

Relevant Graduate Coursework

EECS 470, Computer Architecture (A+)
EECS 583, Advanced Compilers (A+)
EECS 492, Introduction to Artificial Intelligence (A)
EECS 570, Parallel Computer Architecture (A)
EECS 573, Microarchitecture (A+)

Honors and Awards

First-Year Fellowship 2015
EECS Department, University of Michigan
Faculty Scholarship Award 2015
Clemson University
Rhodes Most Outstanding Senior in Computer Engineering Award 2015
ECE Department, Clemson University
Rhodes Most Outstanding Junior in Computer Engineering Award 2014
ECE Department, Clemson University

Skills

Programming Languages: C, C++, Bash, Verilog, VHDL, MATLAB, Java
Tools: GPGPU-Sim, LLVM, Synopsys Design Compiler

Service

Conference Reviewer

- International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES ‘18)
- International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS ‘18)
- International Symposium on Microarchitecture (MICRO ‘17)
- International Symposium on Code Generation and Optimization (CGO ‘17)

Chair of Engineering Futures 08/2014-05/2015
Tau Beta Pi, Clemson University