Self-Assembly for Semiconductor Industry

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Abstract—**Fabrication technologies for the semiconductor industry have enabled ever-smaller devices but now face fundamental limits in creating nanoscale products. Self-assembly has recently emerged as a promising alternative fabrication technology for functional nanoscale systems. Such processes can be made parallel and are capable of producing three-dimensional structures with ~10 nm precision. This paper reviews recent developments, applications and challenges of self-assembly methods for the semiconductor industry. Although a fully self-assembled nanoscale system has not yet been commercially achieved, the work reviewed and discussed here demonstrates a solid scientific foundation in pursuing this goal.**

Index Terms—**Field guidance, lithography, self-assembly, semiconductor manufacturing.**

I. NANOFABRICATION IN SEMICONDUCTOR INDUSTRY

ACHIEVEMENT of short imaging wavelength [1], highly precise imaging optics [2], phase-shifting masks [3], and optical proximity correction [4] all will require dramatic and disruptive technology shifts in the semiconductor industry, in order to continue the pace of achievement set out by Gordon Moore in 1965. Though integrated circuit density and performance have doubled every 18 months [5], the scaling of chip components to less than 22 nm will likely involve a significant role for self-assembly techniques if it has made significant progress by 2010; as such, both validated simulations techniques and experimental demonstrations will be required in order to make self-assembly cost effective. Conventional techniques are generally limited by high cost, insufficient resolution, and limitation to planar fabrication in semiconductor materials. Substrate exposure to corrosive etchants, high-energy radiation, and high temperatures are also problematic in patterning relatively fragile organic materials. Key demands of the future will include parallelizability of processing for speed, nanometer-scale precision, the ability to pattern in multiple environments, preferably outside the clean room and for many types of substrates, and the ability to pattern large areas and 3-D sections, all at low cost.

The present techniques for chip manufacture are listed in order of their usage, along with their limitations, in Table I. Significant capital investments are required with many of these techniques in order to achieve high throughput, high resolution, and low cost.

Among all recently proposed techniques, self-assembly possesses the advantages of allowing patterning the smallest

TABLE I
CAPABILITIES OF CURRENT FABRICATION TECHNIQUES

Techniques	Resolution	Process	Limitation
Photolithography [6]	80 nm	Parallel	High cost, Precision
Scanning beam lithography [10]	10 nm	Serial	Slow rate, Precision
Soft lithography [17]	2 nm	Parallel	Distortion
Scanning probe lithography [20]	1 nm	Serial	Slow rate
Edge lithography [26]	16 nm	Parallel	Restricted structure type
Self-assembly	1 nm	Parallel	Discussed in Section IV

possible size, along with robustness in patterning large areas. However, technical barriers remain for its large-scale implementation. It is instructive to review the progress of the past few decades, and most common manufacturing techniques, in predicting the future of the technology.

Photolithography has dominated as a manufacturing approach in the microelectronics industry since its introduction with the first integrated circuit in 1960s. The predicted lifetime of this approach, given requirements in increased chip capacity, is presently around 10–15 years [6]. Current photolithography has been shown to produce features as small as 30 nm on chips, but smaller features require different types of processes. Proposed methods have included decreasing the imaging wavelength [7], application of extreme ultraviolet (EUV) light [8], or X-rays [9]. All of these require significant capital investments.

Scanning beam lithography, a relatively slower approach to manufacture versus photolithography, is also widely used in chip manufacture, employing either electron or ion beams. Both types are intrinsically serial processes and as such are often used to produce photomasks for projection lithography rather than for actual device fabrication. Fabrication times depend upon the pattern density and feature size; arrays of sub 20 nm features over an area of 1 cm^2 require 24 h. The slow rate of fabrication, high available precision, and high cost of usage and maintenance restrict scanning beam lithography techniques to small areas or low densities of features, primarily in research applications [10]–[12]. Overall, the method can be useful for transistor fabrication and repair, and the ability to write with different ions is potentially useful in tuning the properties of electronic nanostructures.

Unconventional nanofabrication methods that overcome some of the limitations of photolithography and scanning beam lithography, i.e., high capital and operational costs, and/or low resolution, have been developed recently. Soft lithography provides an inexpensive approach to reproduce patterns created by other lithographic means, wherein numerous molds and replicas can be made from the same master [13]–[15]. This technique usually uses elastomeric polydimethylsiloxane (PDMS) stamps with patterned relief on the surface to produce features. The stamps can be prepared by casting polymers against masters patterned with conventional lithographic techniques. Replication of block copolymer templates has led to the fabrication of 20-nm-wide and 27-nm-deep holes [16]. Recently, periodic vertical patterns with peak-to-trough dimension of 1.5 nm have been replicated with PDMS [17]. Distortion or deformation of polymer nanostructures, optimization of conditions for pattern transfer and replication of nanoscale features, and registration of nanoscale features in soft materials for patterning multilayered structures presently limit application of soft lithography [14], [18].

Scanning probe lithography (SPL) is another recent approach for nanofabrication; it uses a conductive scanning probe tip to pattern a thin layer of electron sensitive material and has demonstrated significant potential as an alternative to conventional scanning beam lithography. SPL techniques include scanning tunneling microscopy (STM), atomic force microscopy (AFM), and near-field scanning optical microscopy (NSOM). This technique has shown precise positioning of atoms with an STM tip [19], [20]. Dip-pen nanolithography (DPN) using AFM has produced features as small as 15 nm [21]. Scanning near-field photolithography using NSOM has generated molecular features of 20 nm [22]. The commercial availability of AFM and STM instrumentation and probes makes SPL a convenient approach for nanoscale patterning. However, the inherent serial nature of SPL using a single tip results in undesirably slow writing. Further, SPL lacks the ability to pattern a high density of features over large areas and is also limited to a small set of materials, e.g., thin films of semiconductors, polymers, and some organic molecules. Parallel approaches in SPL are being developed to overcome the serial limitations of standard SPL technologies [23], [24]. However, it is difficult to fabricate an array of functioning probes with high yields and to pattern complex designs by simultaneously addressing each probe.

Edge lithography uses the edge of a topographic feature in the fabrication as well as the developmental stage of nanoscale features [25], [26]. These methods, in which the edges of one pattern become the features of a second pattern, can produce parallel arrays with scale less than 100 nm. There are different forms of edge lithography. One type of approach transfers the edges of a patterned thin film into another material [27]–[29]. A second type converts films that are thin in the vertical direction into structures that are thin in the lateral direction [26], [30]–[32]. Currently, edge lithographic technique is restricted to making certain types of noncrossing line structures that can be achieved in one step. It is also necessary to increase the density of the patterned features over large areas and to establish the electrical connection among individual features.

II. CURRENT DEVELOPMENTS AND OPPORTUNITIES IN NANOSTRUCTURE SELF-ASSEMBLY

A. General State of the Art

Self-assembly, the spontaneous organization of components into larger, well-defined, and stable aggregates [33], could potentially reduce the smallest possible feature size by a factor of two or more over present techniques (Table I). With this technique, elements of the system interact with each other in predefined ways to form spontaneously structures of higher complexity. At the molecular level, this process can lead to 3-D structures with subnanometer precision.

With self-assembly, external forces and geometrical constraints can be exploited to reassemble/reconfigure a system dynamically, on demand, in real materials. These techniques have been demonstrated in monolayers, polymer thin films, and nanoparticle synthesis, discussed in the order as follows.

Self-assembled monolayers (SAM) are single layers of molecules that spontaneously organize into ordered lattice on the surface of a substrate [34]. Various SAMs have been formed using organic molecules on metals [35]–[38] and semiconductors [39]. Recent experiments have shown that a binary inorganic monolayer on an elastic substrate may separate into two phases and self-assemble into ordered patterns, such as triangular lattice of dots, parallel stripes, or serpentine stripes [36], [37], [40]–[44]. The feature size is on the order of 1–100 nm and stable against annealing. Block copolymers are polymers consisting of at least two chemically distinct, immiscible polymer fragments that are joined by a covalent bond [45]. These systems have been shown to develop a variety of regular domain patterns via phase separation [46]–[48]. The size and the period of the structures are typically on the order of 10–100 nm, depending on the conditions of preparation and the relative chain lengths of the participating polymers.

Nanospheres monodisperse in size and shape may self-assemble into thin films of close-packed, ordered lattices. Electric and magnetic fields as well as shear forces and spatial constraints have been used to direct the assembly of nanoparticles and nanorods into different configurations [49]–[51]. The assembly of nanowire arrays is more challenging than that of nanoparticles and nanorods due to their highly anisotropic shape [52], [53]. Nanowire self-assembly usually results in partially ordered, small superlattices. This issue has recently been addressed by several new methods to direct the process, including the use of microfluidic channels and electric fields [54], [55].

B. Opportunities for Use of Self-Assembly Techniques in Semiconductor Manufacturing

The semiconductor industry is presently well-positioned to take advantage of both large and small scale nanoscale self-assembly techniques, as evidenced by demonstrations and the recent availability of simulation tools.

Fig. 1 shows possible applications, along with demonstrations that support further investigations of scale-up in practice of these approaches [56]–[60]. For instance, a polymer layer can create a crystalline template on the chip surface; a nanotextured pattern on silicon can serve as a kind of pegboard
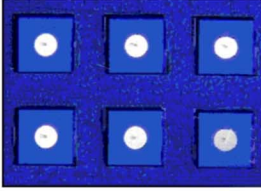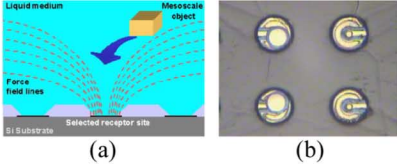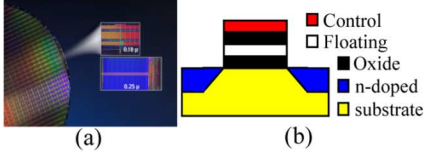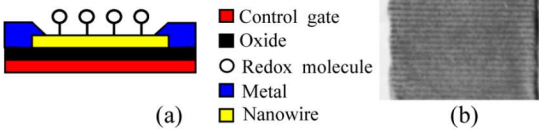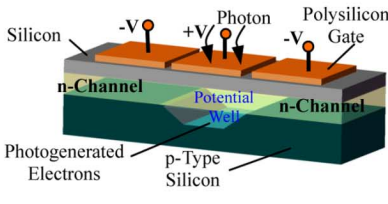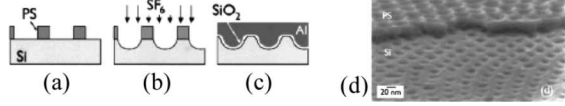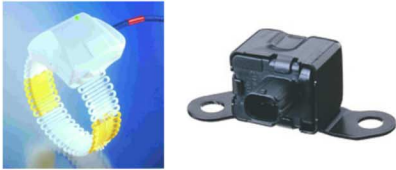
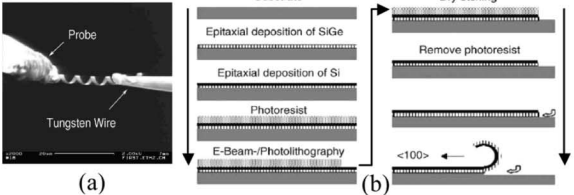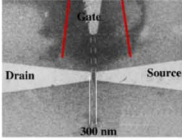| Chip Types	Applications of Self-assembly
LED Chip, 8/9/12 mm, Substrate: GaAs, EML: AlGaInP	(a) Self-assembly driven by a combination of shape recognition and surface tension is used to bind components selectively and provide electrical connectivity. (b) Emitting GaAs LEDs with a diameter of 670 nm seated at selected receptor sites that are pre-patterned on the surface of a silicon chip.
(a) Silicon flash memory. (b) A schematic of the cross-section.	(a) A multilevel molecular memory device based on redox active molecules self-assembled on (b) single-crystal semi-conducting nanowire field-effect transistors.
Metal oxide semiconductor (MOS) capacitor.	Process flow for MOS capacitors. (a) Self-assembled polymer template on silicon surface. (b) RIE pattern transfer of PS template into silicon, followed by the removal of the PS matrix. (c) SiO$_2$ growth followed by the deposition of top Al gate electrode. (d) SEM image after RIE etching.
Electromechanical sensors	(a) Configuration of electromechanical sensors. (b) An initial planar bilayer patterned by conventional microfabrication techniques self-assembles into 3D nanostructure. In the last step, the patterned bilayer curls up along the <100> direction, releasing the internal strain and forming a helical structure during wet etch.
Chip and reader for electrical DNA	An electrical DNA detection method using self-assembled

Fig. 1. Applications of self-assembly. Figures are adopted from [56]–[60].

for attaching components; or, an array of nanoscale silicon pillars can be attachment points for nanoscale capacitor or other components. Nanotubes may be useful at some point, in solving the problem of current leakage encountered by traditional transistors at the nanoscale. Self-assembled polymers can be used as masks, which act like stencils, to create features on silicon wafers able to house active portions of electronic microdevices. Self-assembled polymers can also be used for making lines and spaces, which are useful in the manufacturing of transistors and connecting wires.
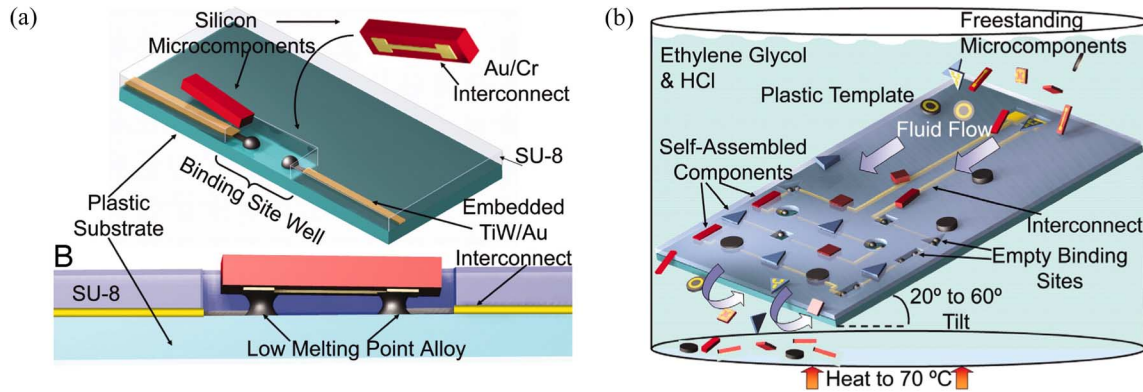
Fig. 2. (a) Fluidic self-assembly using shape-recognition and capillary forces to guide self-assembly. (b) Assembly chamber shows angle at which substrate is tilted and that microcomponents only assemble at complementary shaped recesses. Adapted from [62].

Making nanoscale systems with self-assembly involves the design of internal and external interactions. Internally, the interaction between elements that constitute the final system, such as molecules or particles, is generally controlled using chemistry that involves hydrogen bonding, van der Waals forces, electrostatic forces, or hydrophobic interactions. External forces and geometric constrains can also change the outcome of a self-assembled product and provide additional degrees of freedom. External forces generally have a much coarser scale than atomic distances and can be developed from various physical effects, e.g., elastic, electric, or hydrodynamic interactions.

In present industrial practice, design and implementation of self-assembly are still limited to construction of microscale systems, e.g., use of gravity and hydrodynamic forces to guide components into recesses on a substrate [61]. Gravitational forces [61], shape recognition [62], or capillary forces [63]–[65] are then used to guide the self-assembly of parts onto the binding sites, as shown in Fig. 2. Integration of prefabricated microcomponents onto a substrate at prescribed locations by self-assembly has also been accomplished. In a typical process, microcomponents suspended in a liquid flow past a series of prescribed binding sites on a template. After components are assembled, van der Waals force keeps the components in place for subsequent processing.

This method is currently used in industry as a mass manufacturing scheme, due to its high assembly rate. Shape recognition has also been used to assemble individually p-channel, n-channel, and diffusion resistors in a predetermined manner on a substrate [62].

An approach using capillary force has been demonstrated to accurately position freestanding silicon parts onto a template with submicrometer precision [65]. More complex integrations between multiple types of components and the substrate have been achieved using electrochemical modulation [66]. Assembly of multiple types of components on the same substrate is achieved by electrochemical modulation of the hydrophobicity of specific binding sites. Electrostatic forces demonstrate significant potential in dynamic control of self-assembly since it is easy to manipulate and apply at specific locations. Positioning components have been demonstrated using electrostatic forces [67]. The self-assembly of silicon resistors onto templates has been achieved by the combination of dielectrophoresis and electrohydrodynamics [68]. The surface tension forces can be used to drive and align many microstructures including optoelectronics [69], [70]. A combination of shape recognition and solder surface tension-driven self-assembly was used to bind components selectively and provide electrical connectivity [71]. Fig. 3 shows this process and the experimental demonstration of assembled heterogeneous microsystems.

Self-assembly has recently been demonstrated in the fabrication of 3-D microstructures. Microactuators, microsensors, microcontrollers, and micropower sources have all been integrated into 3-D structures to create complex microstructures or micromachines [72]–[75]. Fig. 4 shows one application, in which polyhedral metal plates were assembled into large arrays using hydrophobic–hydrophilic interactions [76]. Although this approach has not been commercially utilized yet, it demonstrates the potential to grow microstructures and electronic circuits.

Currently, commercial applications of self-assembly in industry have been limited in the integration of microscale components. However, recent studies have revealed the considerable potential of self-assembly in manufacturing nanoscale devices. In the following section, we survey recent progress of applying self-assembly to make nanoscale features and devices.

III. RECENT ADVANCES

Self-assembled monolayers (SAMs) can be used to create well-defined chemical systems in nanoscale devices at target locations. In current molecular electronic structures, a location for the assembly of an SAM is microfabricated. Then, a SAM is allowed to self-assemble onto the correct location in the device structure. Desired functionality is obtained by designing and positioning the proper molecules in the device.

SAMs have been used as molecular memories [58], [77], [78] and molecular wires [79]–[81] and have exhibited negative differential resistance [82]–[84]. They have also been used in integrated circuits and MEMS [85]–[87]. Recently, SAMs have been shown to resolve the stiction problems in MEMS devices [85]. Another application of SAMs is to serve as patterned templates for the self-assembly of nanoscale electronic devices, such as carbon nanotubes [88]–[90]. SAMs also demonstrated significant advantages as resists in lithography, since they can self-assemble onto the substrate with large and very thin surface profiles. SAMs have been patterned by various methods
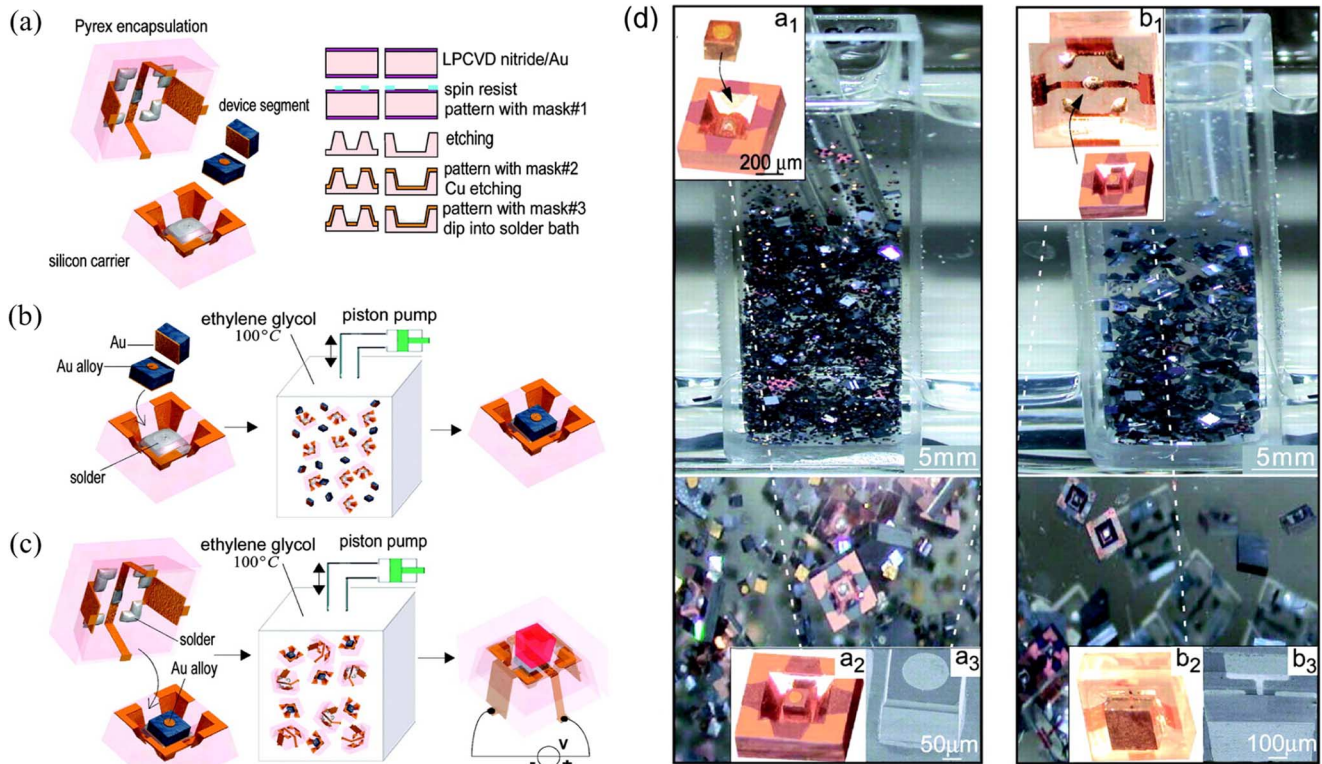
Fig. 3. Fabricating integrated semiconductor devices by sequential shape-and-solder-directed self-assembly. (a) Surface micromaching defines silicon carrier and encapsulation units. (b) Assembly of LED device to silicon carrier. (c) Encapsulation of units. (d) Experimental demonstration. Device components before (a_1 and b_1) and after (a_2 and b_2) each assembly step are shown. Scanning electron micrographs (a_3 and b_3) show alignment between components. Adapted from [71].
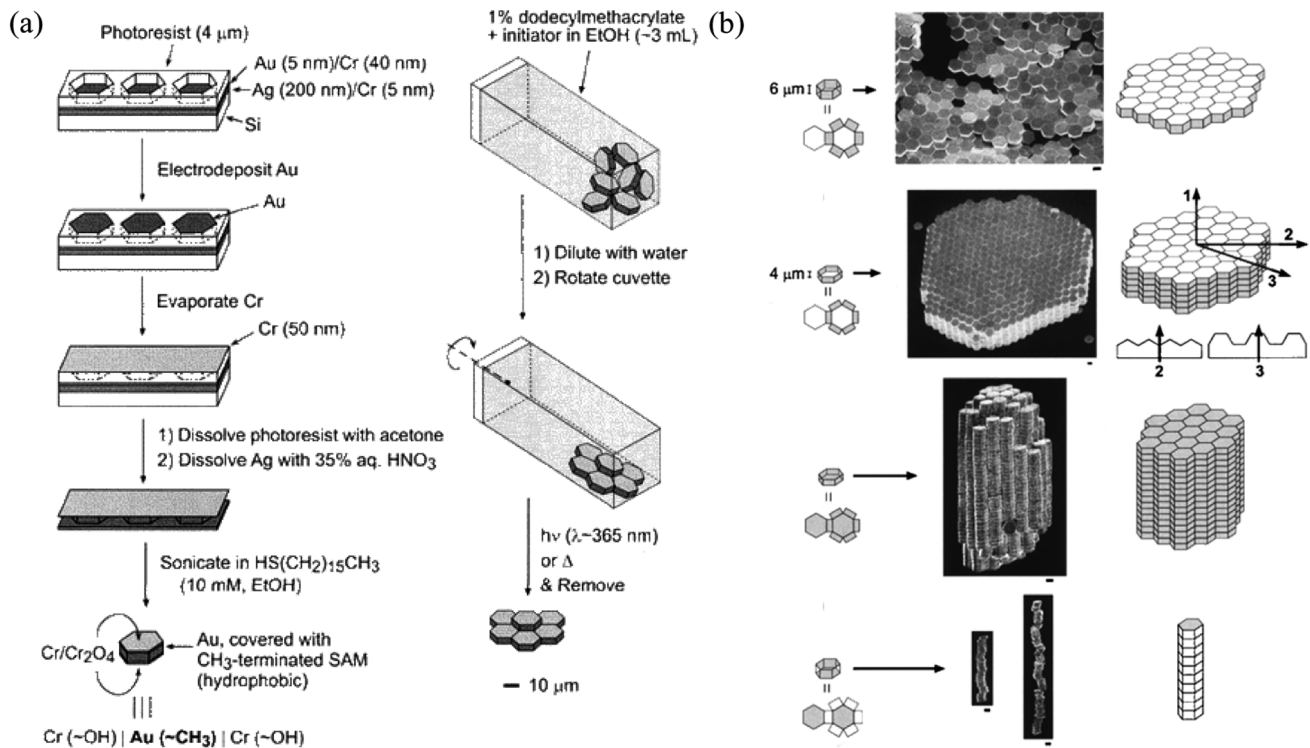
Fig. 4. (a) Fabrication and self-assembly of 10-μm-sized Cr($\sim$OH)$|$Au-($\sim$CH$_3$)$|$Cr($\sim$OH) plates. Plates were fabricated with defined hydrophobic faces and then allowed to self-assemble by depositing hydrophobic liquid on these faces. (b) Various shapes of the resulting self-assembled arrays. They were determined by geometry and pattern of edge/face functionalization of hexagonal plates. Adapted from [76].

[86], [87], [91], [92]. Among them, patterned SAMs by the microcontact printing method have been demonstrated to make printed organic electronic circuits [86], [87].

Fig. 5 shows illustrations of the molecular memory and two organic electronic devices manufactured using SAMs. Templates of SAMs have also been used to mask the deposition

Fig. 5. Illustrations of (a) silicon flash memory and (b) molecular memory for multilevel nonvolatile data storage. (c) In silicon memory cell, four different levels of charges are placed in floating gate via channel hot electron injection. Multilevels of molecular memory are represented by altering population of reduced/oxidized molecules with gate voltage pulses of different amplitude. (d) Microcontact printing of integrated transistors and light emitting diodes. (e) Complementary inverter circuits. Adapted from [58], [86].

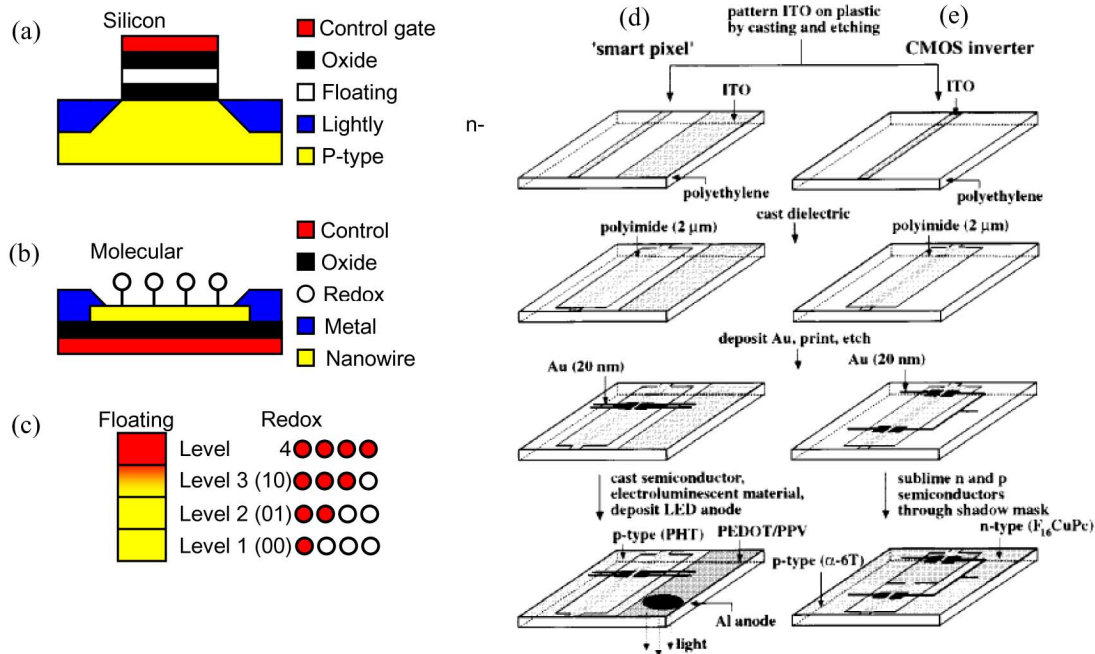of metal [93] or guide the growth of metal nanoparticles [94], [95] and nanowires [96], [97]. The inorganic nanoparticles or nanowires are often fabricated at electrodes and are electrically conductive [98]. Using SAMs to build nanoscale electronic devices or circuits is an intriguing prospect. They can potentially provide the basis for very high-density data storage and high-speed devices.

Self-assembled block copolymers have been used to make nanoscale patterns. In the process, a thin block copolymer self-assembles into ordered patterns on a surface. One phase of the polymer is then selectively removed. The resulting polymer pattern can be transferred to the substrate by various methods, such as dry etching or electroplating. The self-assembly of PS/PMMA in the shape of cylinders perpendicular to a gold surface has been used for the fabrication of nanoelectrodes [99]. Photonic crystals and mechanochromic materials have been made by the self-assembly of bulk block copolymer [100]. Ordered pores in polymers can be used for reversible hydrogen storage [101]. Self-assembled block copolymers have been adopted to enhance the resolution and dimensional control of conventional patterning processes, which helps to overcome the scale limit. For instance, the directed epitaxial self-assembly of block copolymers on lithographically or chemically defined nanopatterned substrates can generate ordered periodic structures at the molecular scale [102]–[105]. These structures have been used as templates to fabricate nanowires [106]–[108], nanoparticle arrays [109], optical waveguide [110], magnetic storage media [111], silicon capacitors [57], and protein resistant surfaces [112]. Self-assembled block copolymers can also be dispersed with photo-addressable segments to achieve multifunctions [113].

Recent studies have revealed the effects of external forces and constraints in controlling a self-assembly process and the struc-

ture. For instance, ordered nanostructures can be obtained by supercritical fluids [114]. The interdomain spacing of microphase-separated nanostructures can be responsive to pressure [115]. Directed self-assembly with external forces provides the possibility to tune the interaction between individual components and position the final assembly at desired locations. Electric fields have been applied to position self-assembled nanowires [55], [116], [117] and control the orientation of self-assembled patterns in a block copolymer blend [118]–[121] or thin polymer film [122].

Both experimental and theoretical studies focusing on controlling the self-assembly of a nanostructure by applying external fields have emerged [123]–[127]. Examples are shown in Fig. 6(a)–(c). A 3-D model has recently been developed to allow the simulation of the entire self-assembly process and electric field design [123]. It was shown that a thin polymer film subjected to an electrostatic field may lose stability at the polymer-air interface, leading to uniform self-organized pillars emerging out of the film surface. With patterned electrodes, parallel stripes replicating an electrode pattern have been obtained. Nanocomposite performance relies on reproducible dispersion and arrangement of nanoparticles, such that the dominant morphology across macroscopic dimensions is nanoscopic. We have shown that electric fields can help to improve the dispersion of nanoplates. A critical electric field strength for exfoliation is predicted. Structural refinement occurs by cleavage through the center of the stack [128].

We have also developed approaches of substrate strain field and surface chemistry to guide the self-assembly process of binary monolayers [124], [125]. Strain distribution can be manipulated by selective oxide inclusion on the silicon wafer, which has been shown to control the location and size of Ge islands [129] and the shape of atomic steps [130]. Fig. 6(d)–(g)
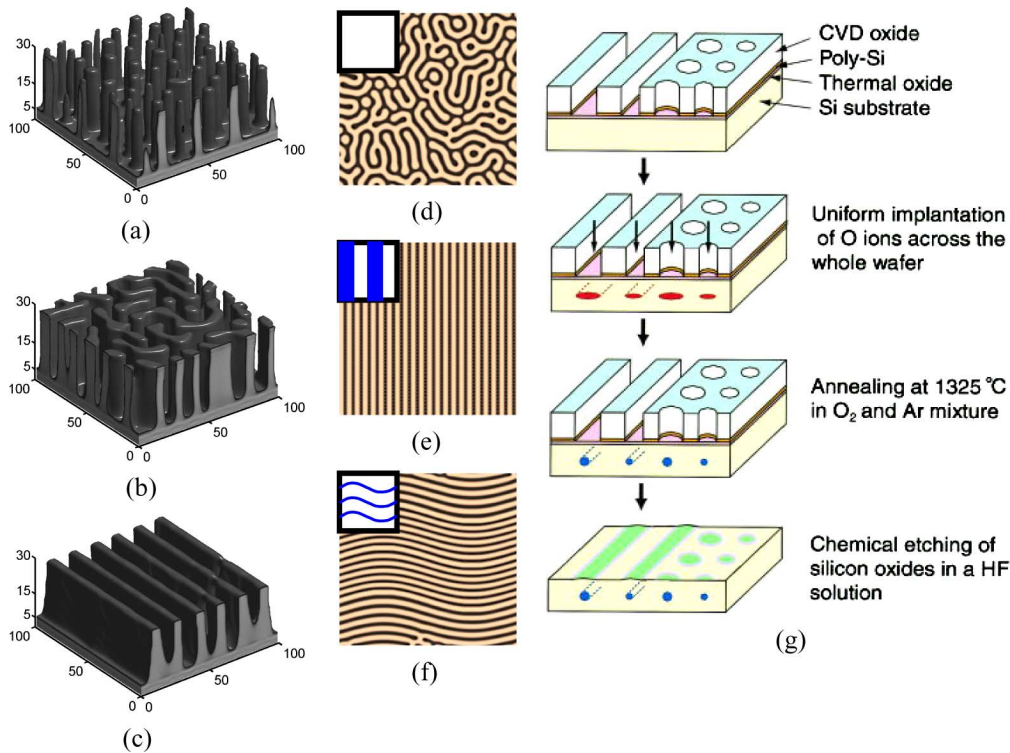
Fig. 6. Various structures developed by applying an electrostatic field to (a) a thin film and (b) a thick film. (c) Designed electric field produces stripe patterns. Self-assembled monolayer patterns guided by substrate strain field: (d) no guidance, (e) strain in blue region, and (f) strain in wavy blue region. (g) Process for producing strain distribution in Si substrates. Adapted from [124], [125], and [129].

shows the guided self-assembly of binary monolayers by surface strain distribution. Prepatterning a substrate with stiff regions and etched spaces can lead to well-controlled nanoc-rack patterns, which can be further filled with various materials to make nanowires [131]. Geometric constraint and magnetic field have also been used to effectively guide self-assembly. The geometric constraints have been used to control the size, shape, and orientation of self-assembled colloidal particles in a microchannel [132], [133]. The structure of photonic crystals consisting of magnetic particles can be tuned by the application of an external magnetic field [134].

Self-assembled quantum dots have the potential for hier-archical control of nanostructures at multiple length scales [135]–[137]. They may serve as the potential building blocks for novel nanoelectronic structures such as quantum cellular automata [138], [139] and circuit elements such as wires, fan-outs, and junctions. Self-assembly plays an important role here since the production of quantum dots over a large area using techniques such as lithography and etching can be expensive and difficult. Modeling and simulations have advanced the fundamental understanding of the self-assembly mechanism and dynamics. Many systems rely on elasticity. For example, both Ge and Si have the same cubic lattice structure, but their lattice constants differ by about 4%. When a Ge film grows on a thick Si substrate, the Ge film strains to match the Si lattice. The elastic energy stored in the film can be reduced if the film breaks into droplets. The shape change is affected by atomic diffusion on the film surface. The resulting droplets have a narrow size distribution and certain spatial ordering. We have recently proposed a self-assembly mechanism for metallic dots without coherent lattice or lattice mismatch with

the substrate, where elasticity is irrelevant. We have shown that electric double layers due to contact potential can lead to size-dependent repulsion, which counterbalances the van der Waal attraction and leads to order nanostructures [140]. The study suggests a possibility of materials selection or application of a bias voltage to the substrate to change the contact potential and thus engineer feature sizes. Nanometer scale metallic dots or clusters grown on a semiconductor substrate have wide applications in optical, electronic, and magnetic devices.

IV. TECHNOLOGY POTENTIALS AND CHALLENGES AHEAD

Beyond its current applications in microscale systems, the potential of self-assembly in nanoscale structures and devices has been demonstrated in a wide range of systems from SAMs to polymers. The products of these self-assembly techniques can be used either directly in a device or indirectly to assist conventional microfabrication processes. Self-assembled poly-mers promise nanoscale feature size, high component density, improved performance, and low voltage requirements for elec-tronic devices. Many of the polymers are commercially avail-able and inexpensive. In addition, the self-assembly of poly-mers can be applied without extraordinary changes in the cur-rent semiconductor manufacturing practices. The materials and processes used are very similar to those employed today in pho-tolithography. Self-assembly offers excellent control over fea-ture size from atomic scale to mesoscales. This characteristic, together with the ability to produce high-density structures in a fast and parallel fashion, is essential to meet the quest for further miniaturization in the semiconductor industry. Although pro-cesses that make use of self-assembly have already produced systems with intriguing functional properties, many challenges

still need to be addressed before the approach can be applied practically and extensively in nanoelecronics industry.

One of the main challenges in self-assembly is the realization of heterogeneous systems with precise dimensional control. The International Technology Roadmap for Semiconductors (ITRS) Emerging Research Materials (EMR) has projected a resolution need of 11 nm. Design rules and approaches need to be developed for material blocks to assemble hierarchically into useful and stable structures, components, devices, and circuits. The second challenge is to develop the capability to precisely produce essential features such as dense and isolated lines/spaces with multiple pitches and sizes in the same layer, as well as shapes such as circles, hexagonal arrays, and contact openings. These features should satisfy low frequency line edge roughness $\sim$2.1 nm 3 σ and gate critical dimension control $\sim$1.7 nm 3 σ. The third challenge is registration between levels, which needs even further work. EMR has projected the overlay and registration need of 5.1–7.1 nm 3σ. The fourth challenge is that self-assembly is prone to producing defects. Due to the thermal fluctuations and the statistical nature of self-assembly in the nanoscale, we anticipate the presence of a finite number of defects in the final assembled structures. Defect management strategies need to be developed to satisfy the requirement of $<$0.02 nm defects/cm^2. Investigating structures insensitive to defects will be essential for designing a system that takes advantage of self-assembly. In terms of throughout, the self-assembly process should be developed to achieve 1 wafer/min. Most of the self-assembled systems from nanoscale components are generally limited to micrometer-sized areas. Working within these constraints is another challenge for device designers and system architectures. Several other challenges include etch resistance to plasma and chemical etches; demonstration of generating sublithographic features ($\sim$5 nm); and demonstration of features doubling the linear density of DUV or EUV lithography. Also, a big challenge is the lack of modeling and simulation tools, which enhance the understanding of the self-assembly mechanisms and translate theory and ideas into devices with optimized performance. Once the mechanisms controlling the self-assembly process are fully understood by well-developed modeling and simulation, the process can be steered to create a wide range of nanostructures for semiconductor industry.

Self-assembly has been employed to make nanoscale electronic devices, memories, and photonic devices in research laboratories. However, most of them remain a research tool. Resolving the challenges in self-assembly will eventually bring this technology from research laboratories to device manufacturing. We anticipate significant development toward the integration of self-assembled nanoscale structures and broad multidisciplinary participation in addressing the current challenges faced by self-assembly. It is believed that in the future self-assembly will be a key approach for nanofabrication.

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