ZhiYoong Foo

zhiyoong@umich.edu
3030 Whisperwood Drive #326 • Ann Arbor, MI, 48105 • (734)272-1460

OBJECTIVE

Ph.D. degree in Electrical Engineering, with long term goals working as an electrical engineer performing circuit design, physical design, or chip integration, with a strong interest in low power and high performance VLSI design with an emphasis on high level of integration of SOCs.

EDUCATION

University of Michigan, Ann Arbor, MI
P.H.D. Electrical Engineering, August 2013
Research Advisor: Professor David Blaauw
B.S.E. Electrical Engineering, December 2006
- Won first place in VLSI I design contest

WORK EXPERIENCE

Research Fellow under Professor David Blaauw and Professor Dennis Sylvester 09/13-Present
University of Michigan, Ann Arbor, MI

- ***Millimeter Scale Wireless Sensor Nodes***
  Development and circuit and systems integration of the millimeter scale wireless sensor nodes with various sensing modalities and transducers. Developed and fabricated over 15 chips through which includes and is not limited to, circuit design, simulation, and layout in Cadence Virtuoso, Verilog design and simulation in Synopsys VCS, synthesis through Synopsys Design Compiler, APR through Cadence Encounter. PCB Board level design and testing was conducted with chips returned from fabrication. Chips were also tested atop a probe station.

Research & Development Intern 08/12-11/12
ARM, San Jose, CA

- ***Memory Power Breakdown***
  Investigated & broke down energy consumption trends in 28nm technology SRAM memory for various bits, words, bank sizes across leaf cell components to understand leading causes of dynamic & leakage power.

Research Assistant under Professor David Blaauw and Professor Dennis Sylvester 01/07-08/13
University of Michigan, Ann Arbor, MI

- ***Developing World Project***
  Developed a low cost audio computer for information dissemination amongst illiterate people groups in 180nm technology. Achieved low cost by using novel memory hierarchy, high level of integration that moved all analog components onto a single chip, and cost aware design decisions at every step. Consists of an ARM Cortex M0, 128kB 4-Way True LRU cache, four Voltage Regulators, a Voltage Step-Up Converter, and a variable Voltage Step-Down/Up Converter, a NAND Flash Controller, a Power On Reset and Brown Out Detector, a Class D amplifier, an 8-input 10-bit ADC, Manchester Encoder/Decoder for near field communication, a 32KHz Crystal driver, two SPI controllers, one UART controller, ten CDCs, a Wakeup-Interrupt Controller, multiple timers, and multiple clock generators. Wrote and verified Verilog connections with Analog components both behaviorally and through circuit instantiations in Nanosim/Ultrasim. Heavily verified all Verilog components and top level integration to ensure functionality. Used Design Compiler and Encounter for top level physical design through pads. Verified physical design for timing closure and functionality.
- ***Commercial Phoenix Processor***
  Designed balloon flip-flops and latches for state retention and several High-Vt cells for use in logic awake during sleep modes for ARM Cortex M0 in 130nm technology. Simulated sleep current of memory banks, processor, and power regulators working at different voltage levels to ensure no sneak leak paths were found.
- ***Swizzle Network***
  Integrated top level in 65nm technology. Wrote Skill to automate large layouts of configurable swizzle switches. Verified analog and digital blocks connectivity through Nanosim with vectors generated from Verilog testbenches with behavioral definitions of analog blocks.
- ***Phoenix Processor***

Produced a complete standard-cell library in 130*nm* technology optimized for use in ultra-low power sensor chips. Designed level converter and comparator cells that enabled low power cells to interface with standard voltage IO.

- ***Oxide Breakdown Detection***
  Implemented a semi-custom FIR filter that incorporated oxide breakdown sensors designed to detect transistor failure in 65*nm* technology. The FIR filter included custom header cells connected to standard gates at various intervals to support transistor failure detection.
- ***Soft Edge Flip-Flop***
  Analyzed the effectiveness of soft edge Flip-Flop design by comparing the performance of traditional and soft edge Flip-Flops. Wrote code that automatically computed max chip performance across bin of chips by tuning clock frequencies and softness of Flip-Flops.
- ***Standard-Cell Library Design***
  Designed a standard-cell library in a 130*nm* technology. Characterized cells using Signalstorm for synthesis by Design Compiler and Auto Place and Route in Encounter.
- ***Graduate Student Instructor***
  Led laboratory and occasional lectures for EECS 427: VLSI I, a course in integrated circuit design.

PUBLICATIONS

1. D. Jeon, Y. Chen, Y. Lee, Y. Kim, Z. Foo, G. Kruger, H. Oral, O. Berenfeld, Z. Zhang, D. Blaauw, D. Sylvester, "An Implantable 64nW ECG-Monitoring Mixed-Signal SoC for Arrhythmia Diagnosis," *IEEE International Solid-State Circuits Conference*, Invited Paper to the *IEEE Journal of Solid-State Circuits*, Special Issue on ISSCC, February 2014
2. Y. Lee, B. Ghiridar, Z. Foo, D. Sylvester, D. Blaauw, "A Sub-nW Multi-stage Temperature Compensated Timer for Ultra-Low-Power Sensor Nodes," *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 10, October 2013, pgs. 2511-2521
3. Z. Foo, et.al., "A Low-cost Audio Computer for Information Dissemination among Illiterate People Groups," Invited Paper to *IEEE Transactions on Circuits and Systems I,* August 2013
4. M. Fojtik, D. Kim, G. Chen, Y. Lin, D. Fick, J. Park, M. Seok, M. Chen, Z. Foo, D. Blaauw, D. Sylvester, "A Millimeter-scale Energy-autonomous Sensor System with Stacked Battery and Solar Cells," *IEEE Journal of Solid-State Circuits*, March 2013.
5. G. Kim, M. Barangi, Z. Foo, N. Pinckney, S. Bang, D. Blaauw, D. Sylvester, "A 467nW CMOS Visual Motion Sensor with Temporal Averaging and Pixel Aggregation," *IEEE International Solid-State Circuits Conference*, February 2013
6. Z. Foo, et.al., "A Low-cost Audio Computer for Information Dissemination among Illiterate People Groups," *IEEE Custom Integrated Circuits Conference*, September 2012.
7. Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, D. Blaauw, "A 660pW Multi-Stage Temperature Compensated Timer for Ultra-Low-Power Wireless Sensor Node Synchronization," *IEEE International Solid-State Circuits Conference,* February 2011.
8. Z. Foo, et.al., "A Case for Custom Silicon in Enabling Low-Cost Information Technology for Developing Regions," *ACM Symposium on Computing for Development*, December 2010.
9. D. Fick, N. Liu, Z. Foo, M. Fojtik, D. Blaauw, D. Sylvester, "In Situ Delay Slack Monitor for High-Performance Processors using an All-Digital, Self-Calibrating 5ps Resolution Time-to-Digital Converter," *IEEE International Solid-State Circuits Conference*, February 2010.
10. G. Chen, M. Fojtik, D. Kim, D. Fick, J. Park, M. Seok, M. Chen, Z. Foo, D. Sylvester, D. Blaauw, "A Millimeter-Scale Nearly-Perpetual Sensor System with Stacked Battery and Solar Cells," *IEEE International Solid-State Circuits Conference*, February 2010.
11. P. Singh, Z. Foo, M. Wieckowski, S. Hanson, M. Fojtik, D. Blaauw, D. Sylvester, "Early Detection of Oxide Breakdown Through In Situ Degradation Sensing," *IEEE International Solid-State Circuits Conference*, February 2010.
12. S. Satpathy, Z. Foo, B. Giridhar, D. Sylvester, T. Mudge, D. Blaauw, "A 1.07 Tbit/s 128x128 Swizzle Network for SIMD Processors," *IEEE Symposium on VLSI Circuits*, June 2010.
13. S. Hanson, Z. Foo, D. Blaauw, D. Sylvester, "A 0.5V Sub-Microwatt CMOS Image Sensor with Pulse-Width Modulation Read-Out," *IEEE Journal of Solid-State Circuits*, April 2010.
14. S. Hanson, M. Seok, Y. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, D. Blaauw, "A Low-Voltage Processor for Sensing Applications with Picowatt Standby Mode," *IEEE Journal of Solid-State Circuits*, April 2009.

15. M. Wieckowski, Y.M. Park, C. Tokunaga, D.W. Kim, Z. Foo, D. Sylvester, D. Blaauw, "Timing Yield Enhancement Through Soft Edge Flip-Flop Based Design," *Proceedings of IEEE Custom Integrated Circuits Conference*, September 2008.
16. M. Seok, S. Hanson, Y.-S. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, D. Blaauw, "The Phoenix Processor: A 30pW Platform for Sensor Applications," *IEEE Symposium on VLSI Circuits*, June 2008.